IN THE CLAIMS

1. (currently amended): A method for manufacturing a semiconductor element using Shallow Trench Isolation, comprising sequential steps of:

~~a step of~~ forming, on a substrate on which a protection oxide film for protecting an active region and a nitride film to be used as an etching stopper are formed in this order, an insulation film for protecting the nitride film;

~~a step of~~ etching the insulation film, the nitride film, the protection oxide film, and the substrate on the semiconductor element separation region to form a trench;

~~a step of~~ etching the insulation film to widen its aperture toward an inside of the active region;

~~a step of~~ performing a heat treatment to form a thermal oxidation film inside the trench;

~~a step of~~ etching the nitride film using the insulation film with the widened aperture as a mask to move a step defined by the thermal oxidation film and the nitride film from an upper edge of the trench toward the inside of the active region;

~~a step of~~ forming a filling oxide film for burying the trench;

~~a step of~~ selectively etching the filling oxide film and the insulation film to expose the nitride film;

~~a step of~~ etching the filling oxide film inside the trench so that a surface of the substrate is substantially level with a surface of the filling oxide film; and

~~a step of~~ removing the nitride film and the protection oxide film.

2. (original): A method for manufacturing a semiconductor element according to claim 1, wherein

the insulation film is an oxide film.

3. (original): A method for manufacturing a semiconductor element according to claim 2, wherein

the selective etching for the filling oxide film and the insulation film is Chemical Mechanical Polishing.

4. (original): A method for manufacturing a semiconductor element according to claim 3, wherein

the nitride film is scarcely etched in the selective etching for the filling oxide film and the insulation film.

5. (currently amended): A method for manufacturing a semiconductor element according to claim 4, wherein

[[the]] an aperture of the insulation film is widened by about 50 nm toward the inside of the active region in the step of widening the aperture of the insulation film toward the inside of the active region.

6. (currently amended): A method for manufacturing a semiconductor element using Shallow Trench Isolation, comprising:

~~a step of~~ forming, on a substrate on which a protection oxide film for protecting an active region and a nitride film to be used as an etching stopper are formed in this order, a polysilicon film for protecting the nitride film;

~~a step of~~ etching the polysilicon film, the nitride film, the protection oxide film, and the substrate on the semiconductor element separation region to form a trench;

~~a step of~~ performing a heat treatment to form a thermal oxidation film inside the trench and to modify the polysilicon film into an oxide film;

~~a step of~~ etching the nitride film using the oxide film as a mask and to move a step defined by the thermal oxidation film and the nitride film from an upper edge of the trench toward the inside of the active region;

~~a step of~~ forming a filling oxide film for burying the trench;

~~a step of~~ selectively etching the filling oxide film and the oxide film to expose the nitride film;

~~a step of~~ etching the filling oxide film inside the trench so that a surface of the substrate is substantially level with a surface of the filling oxide film; and

~~a step of~~ removing the nitride film and the protection oxide film.

7. (original): A method for manufacturing a semiconductor element according to claim 6, wherein

the polysilicon film is replaced by an amorphous silicon film.

8. (original): A method for manufacturing a semiconductor element according to claim 6, wherein the selective etching for the filling oxide film and the oxide film is Chemical Mechanical Polishing.

9. (original): A method for manufacturing a semiconductor element according to claim 6, wherein

the nitride film is scarcely etched in the selective etching for the filling oxide film and the oxide film.

10. (currently amended): A method for manufacturing a semiconductor element using Shallow Trench Isolation, comprising:

~~a step of~~ forming, on a substrate on which a protection oxide film for protecting an active region and a nitride film to be used as an etching stopper are formed in this order, an insulation film for protecting the nitride film;

~~a step of~~ etching the insulation film, the nitride film, the protection oxide film, and the substrate on the semiconductor element separation region to form a trench;

~~a step of~~ performing a heat treatment to form a thermal oxidation film inside the trench;

~~a step of~~ forming an oxide film to be used for forming spacers on a whole surface of the substrate and then forming oxide film sidewall spacers having a step below the substrate surface by etching back the oxide film;

~~a step of~~ forming a filling oxide film for burying the trench;

~~a step of~~ selectively etching the filling oxide film and the insulation film to expose the nitride film;

~~a step of~~ etching the filling oxide film inside the trench and the oxide film sidewall spacers so that the substrate surface is substantially level with a surface of the filling oxide film; and

~~a step of~~ removing the nitride film and the protection oxide film.

11. (original): A method for manufacturing a semiconductor element according to claim 10, wherein

the insulation film is an oxide film.

12. (original): A method for manufacturing a semiconductor element according to claim 11, wherein

the selective etching for the filling oxide film and the insulation film is Chemical Mechanical Polishing.

13. (original): A method for manufacturing a semiconductor element according to claim 12, wherein

the nitride film is scarcely etched in the selective etching for the filling oxide film and the insulation film.

14. (currently amended): A method for manufacturing a semiconductor element using Shallow Trench Isolation, comprising:

~~a step of~~ forming, on a substrate on which a protection oxide film for protecting an active region and a nitride film to be used as an etching stopper are formed in this order, an insulation film for protecting the nitride film;

~~a step of~~ etching the insulation film, the nitride film, the protection oxide film, and the substrate on the semiconductor element separation region to form a trench;

~~a step of~~ performing a heat treatment to form a thermal oxidation film inside the trench;

~~a step of~~ forming a polysilicon film on a whole surface of the substrate to form polysilicon film sidewall spacers on a sidewall of the trench by etching back the polysilicon film, the spacers having a step below the substrate surface;

~~a step of~~ performing a heat treatment to modify the polysilicon film sidewall spacers into oxide film sidewall spacers;

~~a step of~~ forming a filling oxide film for burying the trench;

~~a step of~~ selectively etching the filling oxide film and the insulation film to expose the nitride film;

~~a step of~~ etching the filling oxide film inside the trench and the oxide film sidewall spacers so that the substrate surface is substantially level with a surface of the filling oxide film; and ~~a step of~~

removing the nitride film and the protection oxide film.

15. (original): A method for manufacturing a semiconductor element according to claim 14, wherein

the polysilicon film is replaced by an amorphous silicon film.

16. (original): A method for manufacturing a semiconductor element according to claim 14, wherein

the insulation film is an oxide film.

17. (original): A method for manufacturing a semiconductor element according to claim 16, wherein

the selective etching for the filling oxide film and the insulation film is Chemical Mechanical Polishing.

18. (original): A method for manufacturing a semiconductor element according to claim 17, wherein

the nitride film is scarcely etched in the selective etching for the filling oxide film and the oxide film.

19. (original): A method for manufacturing a semiconductor element according to claim 18, wherein

the thermal oxidation film on a bottom of the trench is scarcely etched in the formation of the polysilicon film sidewall spacers by etching back the polysilicon film.